

21. (Amended) A process for making a semiconductor device comprising the steps of:

providing a substrate having at least one semiconductor layer;
forming an underlayer over the at least one semiconductor layer;
forming a layer of conductive material over the underlayer having a topography that includes a substantially vertical component;
forming an overlayer over the said layer of conductive material;
etching a contact hole in said overlayer and in an overetch amount of the substantially vertical component; and
forming a contact in said contact hole disposed adjacent to and contacting said vertical component.

22. A process as claimed in claim 21 wherein said vertical component defines a localized thick region in the layer of conductive material.

23. A process as claimed in claim 21 wherein said vertical component is a spacer.

24. A process as claimed in claim 21 further comprising the step of forming a structure having an opening therein under said conductive layer and filling said opening with said conductive material to form said vertical component.

25. A process as claimed in claim 21 wherein said conductive layer is a capacitor electrode.

26. (Amended) A process for making a semiconductor device having an improved contact to a conductive layer comprising the steps of:

providing a first layer of material and forming an opening therein, said opening including sidewalls;
forming a layer of a first conductive material on said first layer of material and along the surfaces of said sidewalls of said opening to form a localized thick region;
forming an overlayer of material on said layer of said first conductive material;

etching a contact hole in said overlayer and an overetch amount of said layer of said first conductive material which communicates with said layer of said first conductive material, wherein said overetch amount is an amount necessary to account for variations if forming said first layer of material and said layer of said first conductive material; and substantially filling said contact hole in said overlayer with a second conductive material which differs in composition from said first conductive layer and which contacts said first conductive material.

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(continued)
27. A process as claimed in claim 26 in which said first conductive material forms spacers on said sidewalls of said opening.

28. A process as claimed in claim 27 in which said second conductive material contacts at least said spacers.

29. A process as claimed in claim 26 in which said first conductive material comprises polysilicon and said second conductive material comprises a metal.

30. A process as claimed in claim 26 in which said first layer and said overlayer comprise insulating materials.

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31. (Amended) A process for making a semiconductor device comprising:
providing a substrate having at least one semiconductor layer;
forming a conductive layer over said at least one semiconductor layer having a topography that includes a substantially vertical component;
forming an overlayer over said conductive layer;
forming a contact in said overlayer and in said vertical component disposed adjacent to and contacting said vertical component; and
forming a structure having an opening therein under said conductive layer and filling said opening with said conductive material to form said vertical component.

32. A process as claimed in claim 31 wherein said vertical component defines a localized thick region in the layer of conductive material.

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35. (Amended) A process for making a semiconductor device having an improved contact to a conductive layer comprising:

providing a first layer of material and forming an opening therein, said opening including sidewalls;

forming a layer of a first conductive material on said first layer of material and along the surfaces of said sidewalls of said opening to form a localized thick region, wherein said first conductive material forms spacers on said sidewalls;

forming an overlayer of material on said layer of said first conductive material;

forming a contact hole in said overlayer and in said localized thick region which communicates with said layer of said first conductive material; and

substantially filling said contact hole in said overlayer with a second conductive material which differs in composition from said first conductive layer and which contacts at least said spacers.

36. A process as claimed in claim 35 in which said first layer and said overlayer comprise insulating materials.

40. (Amended) A process for making a semiconductor device comprising:

providing a substrate having at least one semiconductor layer;

forming a conductive layer over the at least one semiconductor layer having a thick region;

forming an overlayer over the conductive layer; and

forming a contact through the overlayer and in the thick region and physically in contact with the thick region.

41. The process of claim 40, wherein forming a conductive layer having a thick region comprises forming a layer of conductive material having a thick region having a width greater than other portions of the conductive layer.

42. The process of claim 40, wherein forming a conductive layer having a thick region comprises forming a layer of conductive material having a thick region having a width greater than other portions of the conductive layer and a depth extending below the other portions of the conductive layer.

43. The process of claim 40, wherein forming a contact comprises etching a tolerable amount of the thick region and forming a contact physically in contact with the thick region at a depth deeper than an upper surface of the thick region.

F1 (concluded)
[Please cancel claims 44, 45 and 46.]

[Please add claims 47 and 48.]

47. (New) A process for making a semiconductor device comprising:
forming a conductive layer having a first thickness over an underlayer;
forming a thick region of said conductive layer having a second thickness greater than said first thickness;
forming an overlayer over said conductive layer; and
forming a contact in said overlayer and in an overetch amount of said thick region.

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48. (New) The process for making a semiconductor device of claim 47 wherein said contact is formed in said overetch amount of said thick region, wherein said overetch amount has a thickness greater than said first thickness.
